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Anderson

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[54] APPARATUS FOR SELECTING, DETECTING AND/OR REPROGRAMMING SYSTEM BIOS IN A COMPUTER SYSTEM

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[51] Int. Cl.[6] G06F 9/44

[52] U.S. Cl. 713/2

[58] Field of Search 395/651, 652, 395/653; 713/1, 2, 100

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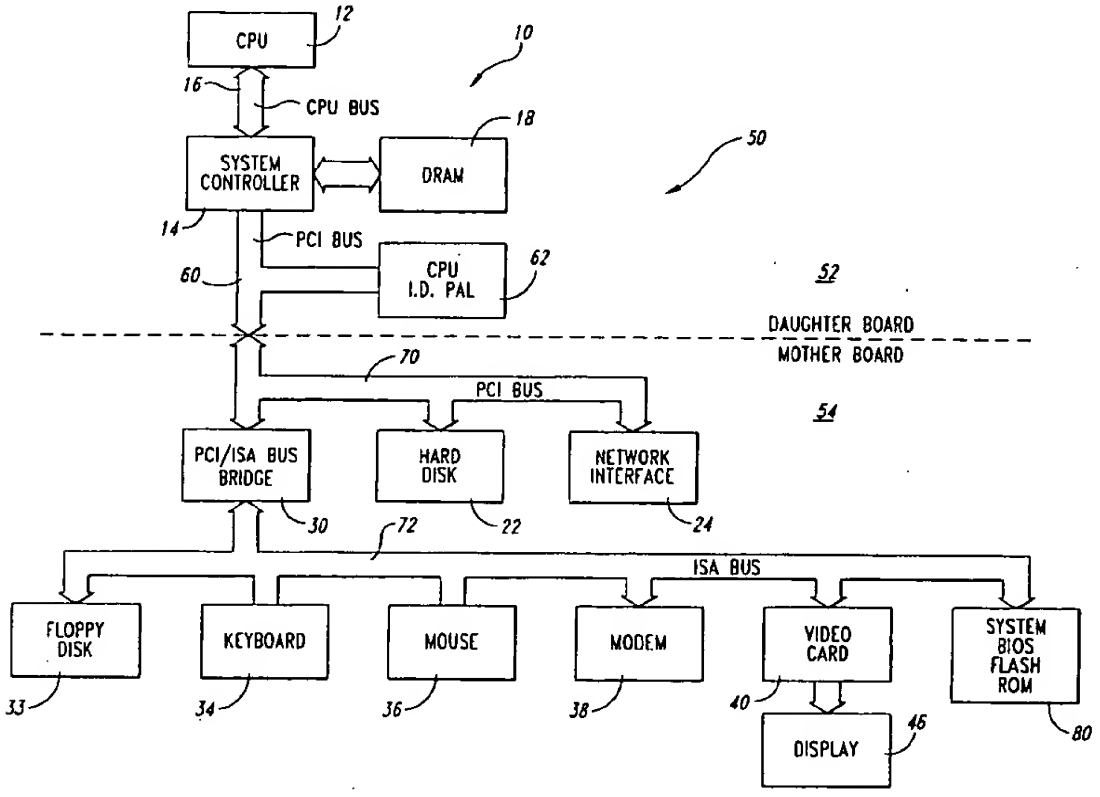
Attorney, Agent, or Firm—Seed and Berry LLP

[57] ABSTRACT

A computer system having a motherboard that is adapted to receive a daughterboard containing a CPU coupled to a PCI bus and a memory device through a system controller. The PCI bus is, in turn, coupled to a storage device, such as a programmable array logic device, containing CPU data identifying the type of CPU or other hardware installed on the daughterboard. The motherboard includes a memory device storing a BIOS program as well as a startup program. The startup program is executed by the CPU at power up or reset to cause the CPU to compare the CPU data identifying the CPU to BIOS data identifying the CPU adapted to execute the BIOS program. In the event that the CPU data and the BIOS data match, the CPU executes the BIOS program in a normal manner. In the event the CPU data does not match the BIOS data, the CPU executes a crisis recovery routine which may involve writing the proper BIOS program from a floppy disk to a programmable memory device containing the BIOS program on the motherboard. The CPU can then execute the proper BIOS program from the programmable memory.

43 Claims, 4 Drawing Sheets



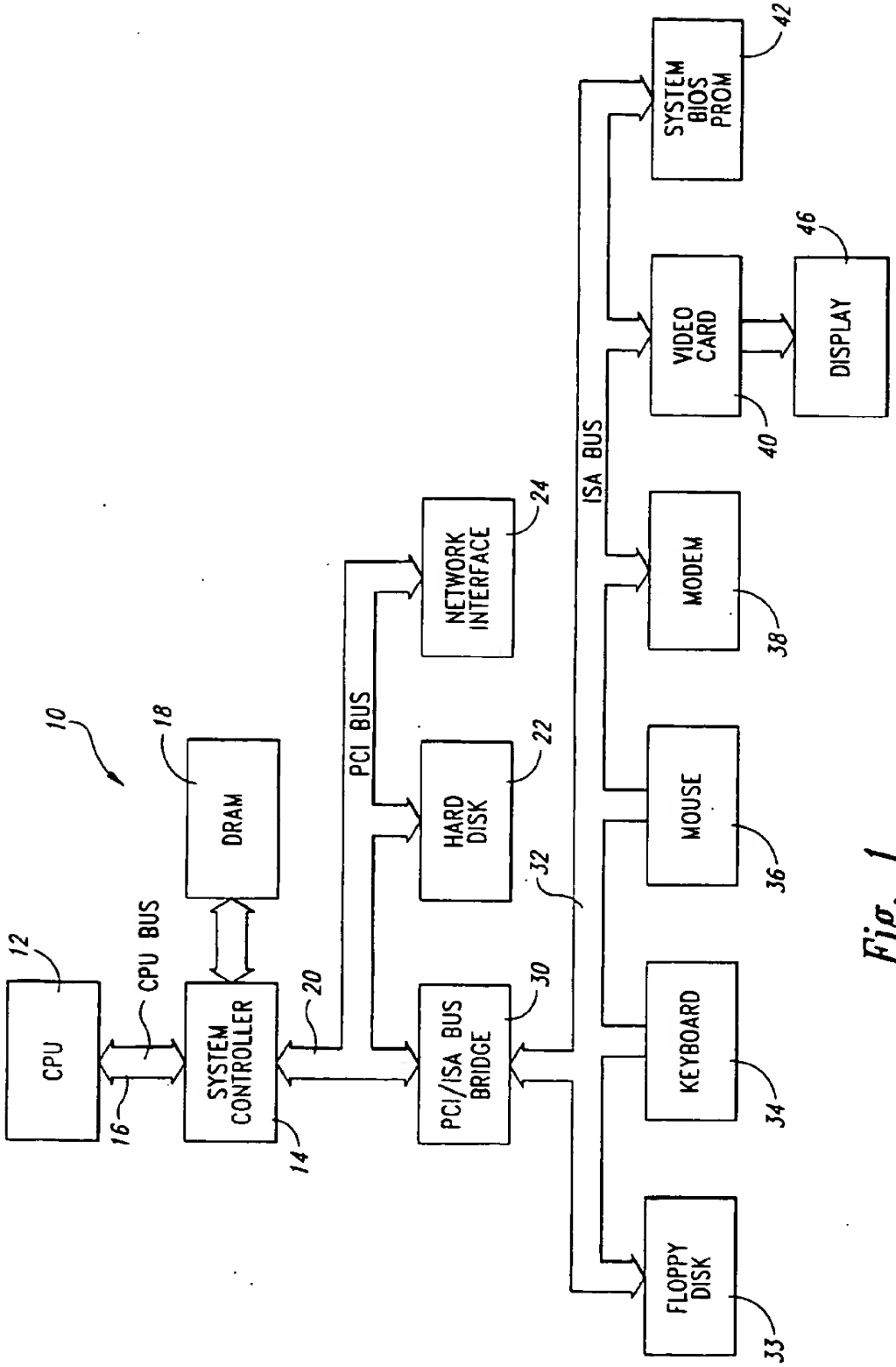


Fig. 1
(Prior Art)

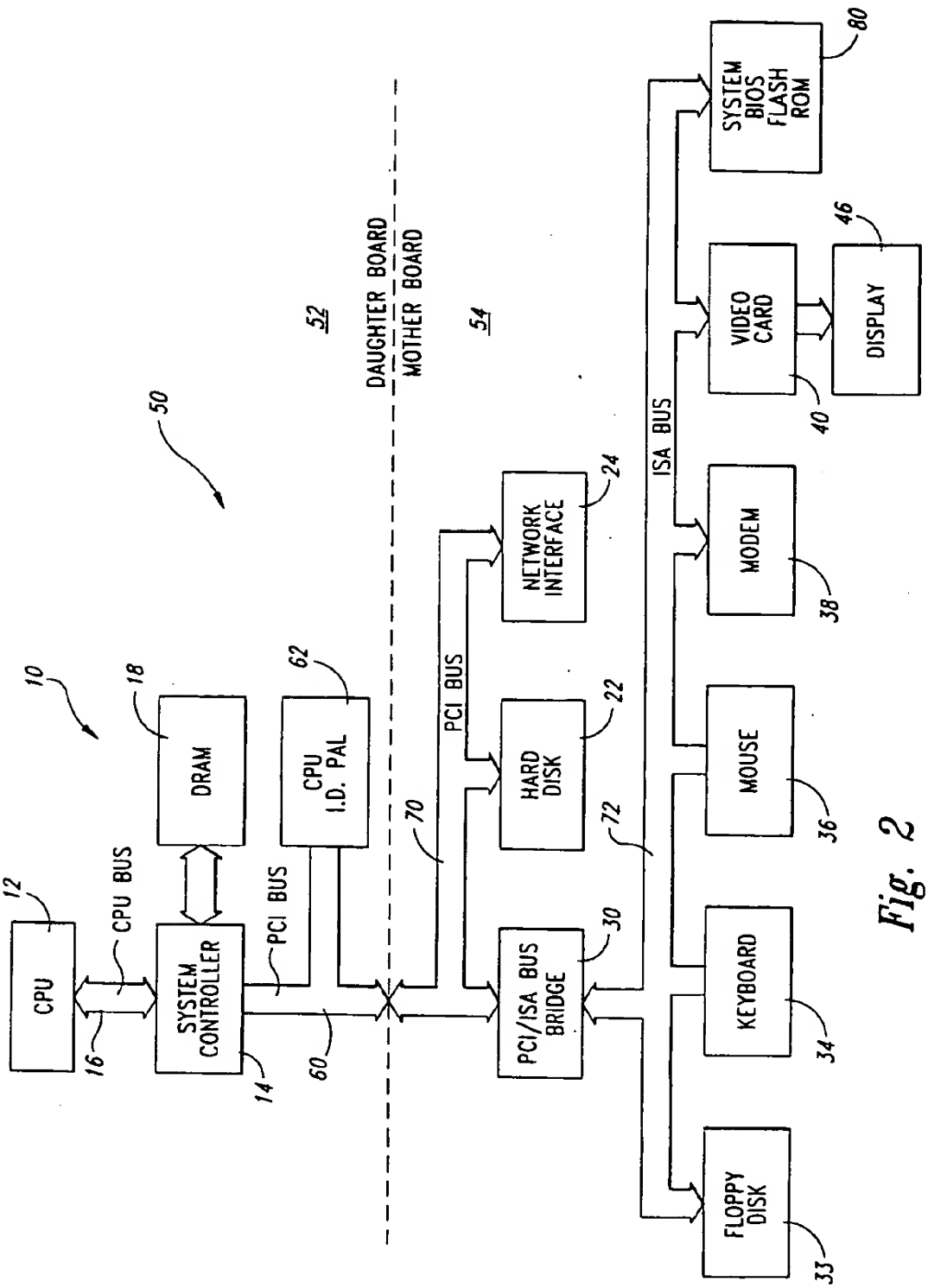

50
10
52
54
DAUGHTER BOARD
MOTHER BOARD
CPU
12
CPU BUS
16
SYSTEM CONTROLLER
14
DRAM
18
PCI BUS
60
CPU I.D. PAL
62
70
PCI BUS
NETWORK INTERFACE
24
HARD DISK
22
PCI/ISA BUS BRIDGE
30
72
ISA BUS
SYSTEM BIOS FLASH ROM
80
VIDEO CARD
40
DISPLAY
46
MODEM
38
MOUSE
36
KEYBOARD
34
FLOPPY DISK
33

Fig. 2

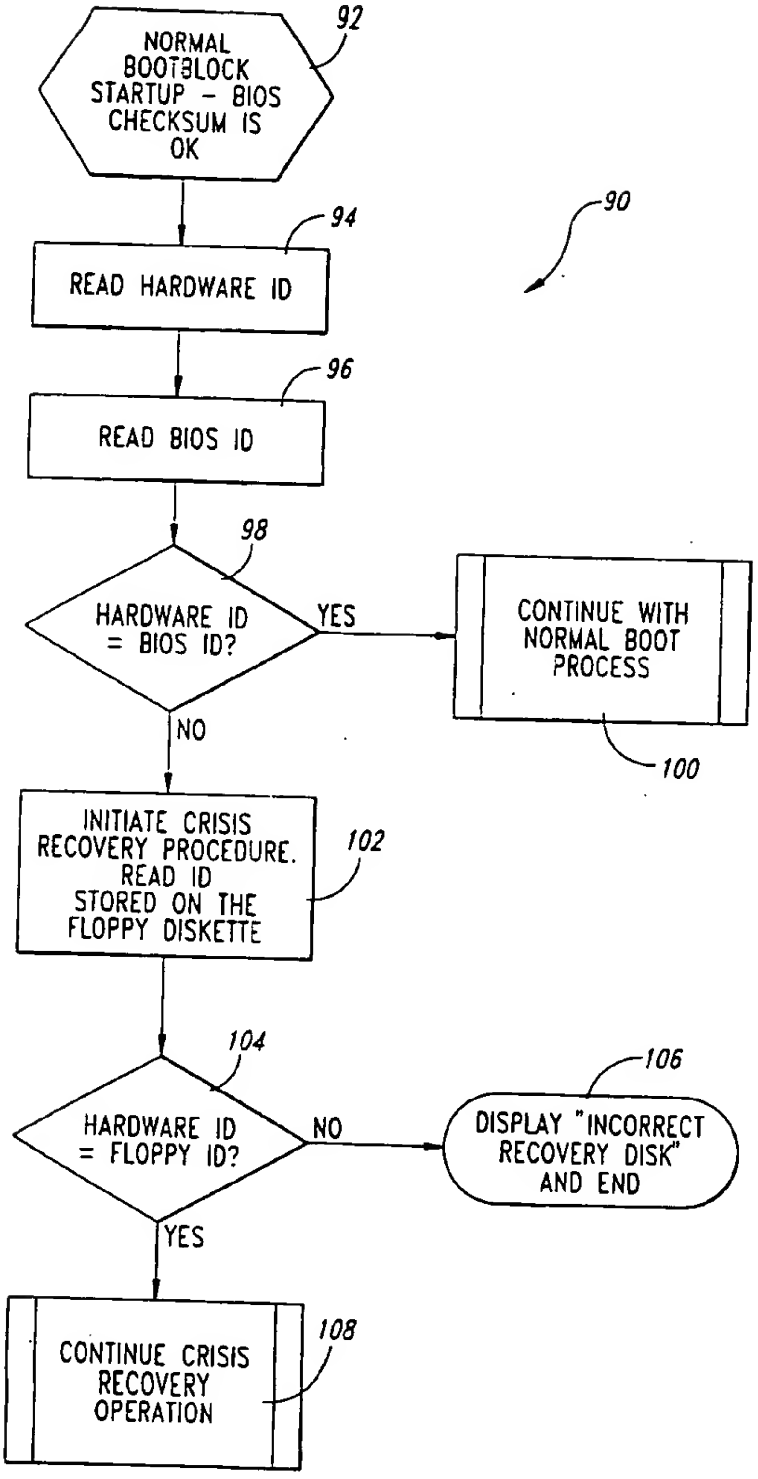

NORMAL BOOTBLOCK STARTUP – BIOS CHECKSUM IS OK
92
90
READ HARDWARE ID
94
READ BIOS ID
96
HARDWARE ID = BIOS ID?
98
YES
CONTINUE WITH NORMAL BOOT PROCESS
100
NO
INITIATE CRISIS RECOVERY PROCEDURE. READ ID STORED ON THE FLOPPY DISKETTE
102
HARDWARE ID = FLOPPY ID?
104
NO
DISPLAY "INCORRECT RECOVERY DISK" AND END
106
YES
CONTINUE CRISIS RECOVERY OPERATION
108

Fig. 3

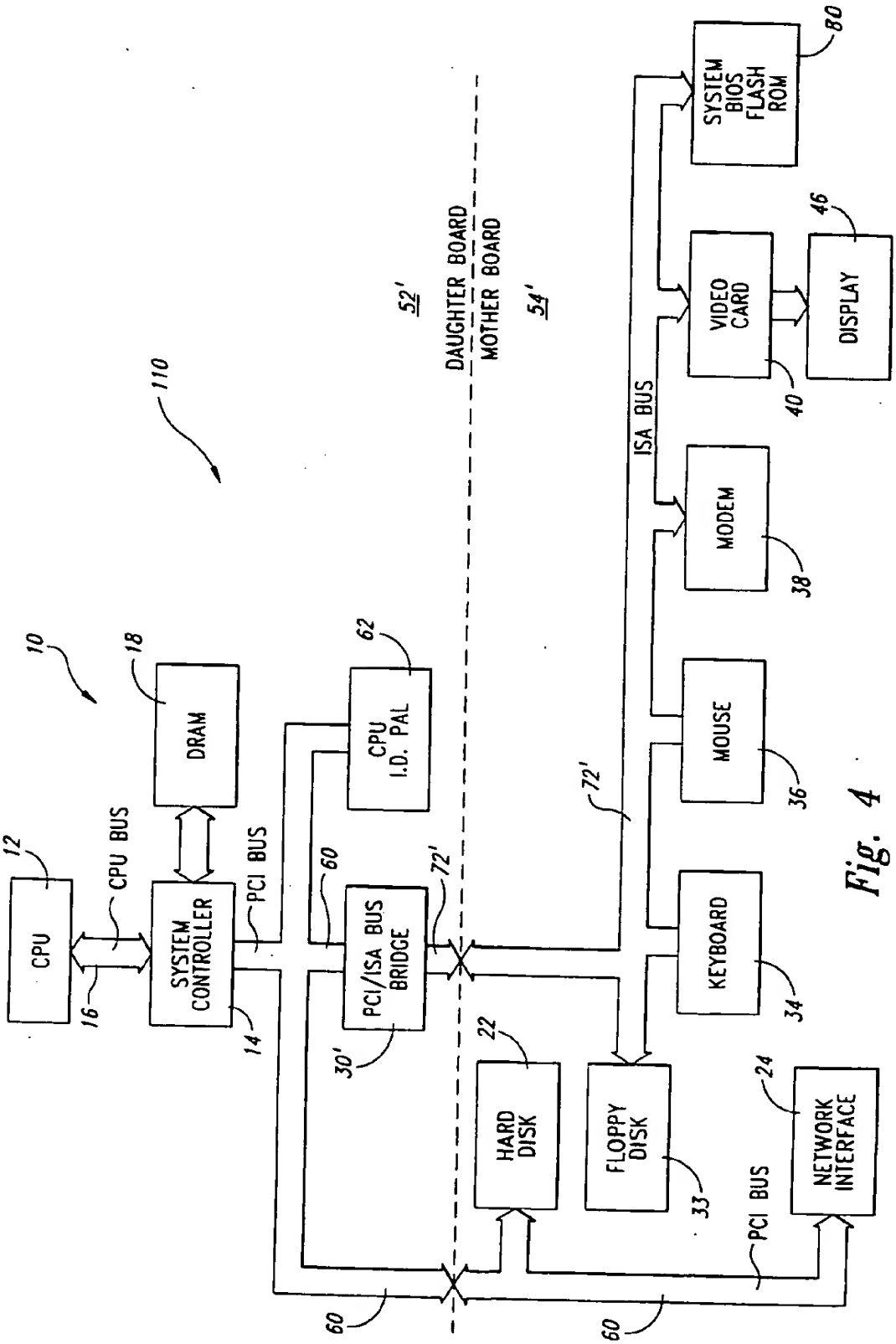

110
10
CPU
12
CPU BUS
16
SYSTEM CONTROLLER
14
DRAM
18
PCI BUS
60
CPU I.D. PAL
62
PCI/ISA BUS BRIDGE
30'
72'
DAUGHTER BOARD
52'
MOTHER BOARD
54'
ISA BUS
72'
SYSTEM BIOS FLASH ROM
80
VIDEO CARD
40
DISPLAY
46
MODEM
38
MOUSE
36
KEYBOARD
34
HARD DISK
22
FLOPPY DISK
33
NETWORK INTERFACE
24
PCI BUS
60
60

Fig. 4

APPARATUS FOR SELECTING, DETECTING AND/OR REPROGRAMMING SYSTEM BIOS IN A COMPUTER SYSTEM

TECHNICAL FIELD

This invention relates to computer systems, and more particularly to a computer system having means for verifying that a selected system BIOS is the correct BIOS for the computer system, for selecting the correct BIOS from among multiple BIOS programs, and for reprogramming a storage device with the correct BIOS if the correct BIOS is not present in the computer system.

BACKGROUND OF THE INVENTION

Personal computer systems are today in wide spread use. The basic architecture of such computer systems has evolved into a relatively common design illustrated in FIG. 1. More specifically, personal computer systems **10**, as illustrated in FIG. 1, include a central processing unit ("CPU") **12**, which may be a microprocessor such as an Intel Pentium® microprocessor. The CPU **12** is connected to a system controller **14** through a CPU bus which normally includes a data bus, an address bus, and a control and status bus. The system controller **14** couples the CPU **12** to a system memory, such as a dynamic random access memory ("DRAM") **16**. Typically, the system controller is coupled to the DRAM **16** through various addressing and control lines. A data bus of the DRAM **16** is connected directly to the data bus of the CPU bus **16**. However, other configurations may also be used.

The system controller **14** also couples the CPU bus **16** to a relatively high speed bus, such as a peripheral component interconnect ("PCI") bus **20**. The PCI bus **20** is coupled to various peripheral devices, such as a hard disk **22** and a network interface device **24**, which may be a local area network ("LAN") card. The PCI bus **20** may also be coupled to other peripheral devices which are not shown in FIG. 1 for purposes of brevity and clarity.

The PCI bus **20** is also coupled through a PCI/ISA bus bridge **30** to a relatively low speed bus, such as an industry standard architecture (ISA) bus **32**. The ISA bus **32** is coupled to a wide variety of peripheral devices, such as a floppy disk drive **33**, a keyboard **34**, a mouse **36**, a modem **38**, a video card **40**, and a programmable read-only memory ("PROM") **42**. The video card **40** is, in turn, connected to a display **46**, such as a cathode ray tube ("CRT") monitor.

As with the PCI bus **20**, a wide variety of other peripheral devices may be connected to the ISA bus **32**. Also, peripheral devices connected to the ISA bus **32**, such as the modem **38** and the PROM **42**, may be instead connected to the PCI bus **20**. Finally, other components typically used in personal computer systems **10**, such as cache static RAM ("SRAM") memory, interrupt handlers, and various control circuitry for the CPU **12**, have been omitted for purposes of clarity and brevity.

In operation, when power is initially applied to the computer system **10**, the CPU **12** accesses a specific memory address in the address space of the PROM **42**. The CPU **12** then starts executing a basic input/output system ("BIOS") program stored in the PROM **42**. The BIOS program stored in the PROM **42** causes the CPU **12** to execute a power-on self test ("POST") program and to then load an operating system that is typically stored on the hard disk **22**. Once the operating system has been executed by the CPU **12** and stored in the system memory **18**, the CPU **12** can execute various application programs, as well known to one skilled in the art.

In practice, the architecture of the computer system raises several issues concerning the selection and/or execution of the BIOS program. For example, the computer system chip set, including all of the components shown in FIG. 1, are generally mounted on a motherboard, although individual components, such as the CPU **12**, may be individually removable from the motherboard (not shown). However, since the PROM **42** and CPU **12** are mounted on a common motherboard, the BIOS program stored in the PROM **42** is assuredly the correct BIOS program for the chip set, including the particular CPU **12** included in the chip set. The computer system **10** shown in FIG. 1 might not operate satisfactorily if the CPU **12** or other chip set component was replaced with a variety of CPU's or other chip set components that did not correspond to the particular BIOS program stored in the PROM **42**. In particular, the BIOS program stored in the PROM **42** may not be the correct BIOS program for the CPU **12** or the correct BIOS program for other components of the chip set. As a result, to the extent that CPUs **12** or other chip set components have been removable from motherboards, they generally may be replaced by only the same type of CPU or chip set component so that they will properly function with the particular BIOS program stored on a PROM **42** or similar device on the motherboard. However, it would be desirable to be able to use different CPUs **12** or other chip set components on a common motherboard for a variety of reasons. For example, it would be desirable to allow different CPUs **12** or other chip set components to be placed on a common motherboard to specially adapt the computer system **10** to various uses. Also, it would be desirable to allow a different CPU **12** or other chip set component to be placed on the motherboard to upgrade the computer system **10** as new devices became available. Unfortunately, if the BIOS program is stored in a memory device mounted on the motherboard, there is no way to ensure correspondency between the BIOS program and the new CPU or other chip set components. It would therefore be desirable to allow various CPUs or other chip set components to be installed on a motherboard even though the BIOS for the CPU or other chip set component is contained in a memory device that remains installed on the motherboard.

Another issue raised by the architecture of computer systems is ensuring that the proper BIOS program is executed in computer systems having more than one BIOS program retained in a storage device. For example, the computer system may have several BIOS programs retained in a storage device, yet the CPU may be capable on executing only one of the BIOS programs, or the BIOS program may be specially adapted for optimum performance with a specific chip set. Under these circumstances, it is necessary to verify that the proper BIOS program has been selected for execution, and, if not, either select a different BIOS program or input the proper BIOS program into the computer system. However, computer system have heretofore not accomplished these functions.

SUMMARY OF THE INVENTION

The inventive computer system includes a central processing unit ("CPU"), and it may also include other chip set components such as a storage device containing hardware data identifying the CPU or other chip set components. The computer system also includes a memory device containing a basic input/output system ("BIOS") program and BIOS identifying data specifying the CPU or other chip set components corresponding to the BIOS program, i.e., the CPU that the BIOS program was designed to be executed by or

the chip set components that the BIOS program was designed to operate with. A startup program, preferably stored in the same memory as the BIOS program, is also adapted to be executed by the CPU. The startup program causes the CPU to read the hardware data from the storage device and the BIOS identifying data from the memory device. The startup program then causes the CPU to compare the hardware data to the BIOS identifying data and, in the event that the hardware data and the BIOS identifying data do not correspond to the same CPU or other chip set components, to either select another BIOS program (if more than one is stored in the computer system) or cause the CPU to execute a crisis recovery routine. The crisis recovery subroutine prompts a user to insert a disk containing the correct BIOS program into a disk drive so that the correct BIOS program can be transferred to programmable memory in the computer system. Rather than comparing stored hardware data with the BIOS identifying data, the computer system may record the BIOS identifying data corresponding to the BIOS program that was last executed by the CPU, and then compare the stored hardware data with the recorded BIOS identifying data.

The ability to verify that the correct BIOS program is to be executed by the CPU and, if not, to take corrective action, allows a chip set containing the CPU and other components to be mounted on a daughterboard that removably plugs into a motherboard containing the remaining components of the computer system. The chip set components mounted on the daughterboard may include a system controller connected to a CPU bus of the CPU, and a system memory coupled to the CPU through the system controller. A relatively high speed bus, such as a PCI bus, may also be coupled to the CPU bus through the system controller. If so, the PCI bus is coupled to the motherboard which may contain a bus bridge to couple the PCI bus to a relatively slow bus, such as an ISA bus. The memory device containing the BIOS program is preferably programmable so that it may be reprogrammed as a function of the specific CPU or other hardware installed in the daughterboard. The memory device may also contain several different BIOS programs, one of which is selected by the startup program as determined by the CPU data.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a conventional computer system.

FIG. **2** is a block diagram of a preferred embodiment of the inventive computer system.

FIG. **3** is a flowchart of the startup program executed by the CPU.

FIG. **4** is a block diagram of an alternative embodiment of the inventive computer system.

DETAILED DESCRIPTION OF THE INVENTION

A computer system **50** according to a preferred embodiment of the invention includes a daughterboard **52** that plugs into a motherboard **54** preferably in a conventional manner. The daughterboard **52** and motherboard **54** contain many components that are common to the prior art computer system **10** illustrated in FIG. 1. These common components have therefore been provided with the same reference numeral, and a description of the function and operation for some of these components may be omitted for purposes of brevity and clarity. Also, the daughterboard **52**, as well as the motherboard **54**, may contain a wide variety of other chip set components which are not shown or described herein for purposes of brevity.

The daughterboard **52** includes the CPU **12** connected to a DRAM **18** through a system controller **14**. The system controller **14** also connects the CPU bus **16** to a PCI bus **60**. The PCI bus **60** is connected to a programmable array logic ("PAL") device **62** which contains data identifying the specific CPU **12** or other hardware installed on the daughterboard **52**. However, other devices, such as read-only memories (not shown), may be used instead of the PAL **62** to store the hardware data identifying the specific CPU **12** or other chip set components installed on the daughterboard **52**.

The PCI bus **60** is also coupled to a PCI bus **70** on the motherboard **54**. As in the computer system **10** of FIG. **1**, the PCI bus **70** is coupled to a hard disk **22**, a network interface device **24**, and a PCI/ISA bus bridge **30**. The ISA bus **72** is then coupled to the keyboard **34**, mouse **36**, modem **38**, and a video card **40** in the same manner as in the conventional system **10** of FIG. **1**. The video card **40** drives a conventional display **46**. The ISA bus **72** is also connected to an electrically erasable programmable read-only memory ("EEPROM") **80** which stores the system BIOS program. The EEPROM **80** is preferably a conventional flash memory device, but other non-volatile memory devices may also be used. Also, although the memory device is preferably programmable, it need not be programmable, and it may store the BIOS programs written for several different CPUs **12** or other chip set components. However, since the daughterboard containing the CPU **12** and other chip set components is removable from the motherboard **54**, there is no assurance that the BIOS program stored in the EEPROM **80** is of the type that is to be executed by the specific CPU **12** contained on the daughterboard **52** or to operate with a specific set of chip set components.

In accordance with the preferred embodiment of the invention, upon reset or power up of the CPU **12**, the CPU **12** executes a startup routine that is also stored in the EEPROM **80** along with the BIOS program. However, it will be understood that the startup program could be stored in a memory device different from the EEPROM **80**. The startup routine must be generic to all CPU's and other chip set components regardless of whether the correct BIOS program is stored in the EEPROM **80** since it must be executed by the CPU **12** to determine if the correct BIOS has been selected for execution by the CPU **12**.

The startup routine will now be explained with reference to the flowchart of FIG. **3**. The startup routine **90** is entered at step **92** in which the CPU **12** executes a number of conventional power-on self tests, including a checksum test of the BIOS program stored in the EEPROM **80**. The CPU **12** then executes step **94** in which it reads the hardware identifying data from the PAL **62**. Similarly, the CPU **12** reads data from the EEPROM **80** at step **96** in order to identify the BIOS program and determine which CPU is adapted to execute the BIOS program. The program then checks at step **98** to determine if the hardware data and the BIOS identifying data correspond to the same CPU or other chip set components, i.e., the CPU **12** is able to execute the BIOS program stored in the EEPROM **80** or the chip set components are able to operate with the BIOS program stored in the EEPROM **80**. If so, the CPU **12** continues with the normal boot process at step **100**. If not, the CPU **12** executes a crisis recovery procedure at step **102**. As is known in the art, the crisis recovery routine prompts the user to install a disk containing the proper BIOS program on the floppy disk drive. Although the user is preferably prompted to install the disk by reading a message on the display **46**, it will be understood that the display **46** may not be operable because the BIOS program has not been executed. Under

these circumstances, the user can be prompted by other means, such as by energizing a beeper (not shown) or flashing a light emitting diode ("LED") (not shown).

With continued reference to FIG. 4, at step 104, the CPU 12 reads data identifying the CPU or other chip set components corresponding to the boot program on the floppy disk and compares it to the hardware data from the PAL 62. If the floppy disk does not contain the correct BIOS program for the CPU 12 or other chip set components, the CPU 12 causes an "Incorrect Recovery Disk" message to be displayed on the display 46 at step 106. If the correct BIOS program is stored on the floppy disk, the CPU 12 continues with the normal crisis recovery operations through step 108. These normal crisis recovery operations may, but not necessarily, include writing the proper BIOS program into the EEPROM 80. Thereafter, the CPU 12 can boot up in the normal fashion through steps 92–100 at power-on.

By including a startup routine that allows the system to determine if the BIOS program stored on the motherboard can be executed by the CPU or work with other chip set components on the daughterboard 52, the computer system 50 is able to accept daughterboards containing a variety of CPUs 12 and other chip set components. Further, the EEPROM 80 may contain several BIOS programs, each of which is specifically adapted to be executed by a respective CPU type or work with a specific set of chip set components. Instead of simply comparing the hardware data to the BIOS identifying data at step 98, the CPU 12 can select a BIOS program corresponding to a specific CPU or chip set, and the selected BIOS program is then used in the normal boot process at step 100. Thus, the computer system 50 is able to accept daughterboards containing a wide variety of CPUs 12 or other chip set components.

An alternative embodiment of the inventive computer system is illustrated in FIG. 4. Most of the components of the system 110 illustrated in FIG. 4 are identical to the components of the computer system 50 illustrated in FIG. 2. These components have therefore been provided with the same reference numerals, and a description of their structure and operation will not be repeated in the interest of brevity and clarity. The computer system 110 shown in FIG. 4 differs from the computer system 50 of FIG. 2 by placing the PCI/ISA bus bridge 30 on the daughterboard 52' rather than on the motherboard 54'. Thus, in the embodiment illustrated in FIG. 4, the daughterboard 54' includes an ISA bus 72' as well as a PCI bus 60. Both the PCI bus 60 and the ISA bus 72' are then coupled to the motherboard 54. The PCI bus 60 and the ISA bus 72' are then coupled to the same components shown in FIG. 2 in the same manner.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. For example, although the preferred embodiment of the inventive computer system is explained primarily as allowing a mother board to removably receive daughterboards containing CPU's or other chip set components, it will be understood that the invention is applicable to compter systems not having removable daughterboards. For example, a computer system could be configured differently for different customers or different applications, with hardware data stored in the PAL 62 identifying the customer or application. The preferred embodiment of the inventive computer system would then compare the hardware data to the BIOS identifying data stored in the EEPROM 80 to either verify that the correct BIOS program had been selected for execution by the CPU. If the correct BIOS program had not been selected, the CPU could either select a different BIOS program (if several were stored in the computer system) or execute a crisis recovery routine. These and other modifications of the preferred embodiment of the invention will be apparent to one skilled in the art. Accordingly, the invention is not limited except as by the appended claims.

I claim:

1. A computer system comprising:

a first circuit component including at least a central processing unit ("CPU") and a storage device containing system data identifying hardware or software in the first circuit component; and

a second circuit component removably receiving the first circuit component, the second circuit component including a memory device containing a basic input/output system ("BIOS") program, BIOS identifying data corresponding to the BIOS program, and a startup program adapted to be executed by the CPU to cause the CPU to read the system data from the storage device and the BIOS identifying data from the memory device, compare the system data to the BIOS identifying data, and, in the event the system data and the BIOS identifying data do not correspond to each other, cause the CPU to automatically execute a crisis recovery routine that allows loading of an alternative BIOS program.

2. The computer system of claim 1 wherein the first circuit component comprises a circuit board having the CPU and a storage device containing the system data mounted thereon.

3. The computer system of claim 1 wherein the CPU includes a CPU bus, and wherein the first circuit board further comprises a system memory and a system controller specifically adapted to interface with the CPU, the system controller coupling the CPU bus to the system memory.

4. The computer system of claim 1 wherein the first circuit component further comprises a CPU bus coupled to the CPU, a relatively high speed bus, a system memory, and a system controller specifically adapted to interface with the CPU, the system controller coupling the CPU bus to the system memory and to the relatively high speed bus.

5. The computer system of claim 4 wherein the relatively high speed bus comprises a peripheral connect interface ("PCI") bus.

6. The computer system of claim 1 wherein the first circuit component further comprises a relatively high speed bus coupled to the CPU, and wherein the second circuit component further comprises a relatively high speed bus removably coupled to the relatively high speed bus of the first circuit component.

7. The computer system of claim 1 wherein the first circuit component further comprises a relatively high speed bus coupled to the CPU, and wherein the second circuit component further comprises a relatively high speed bus removably coupled to the relatively high speed bus of the first circuit component, a relatively low speed bus, and a bus bridge coupling the relatively high speed bus to the relatively low speed bus.

8. The computer system of claim 7 further comprising a plurality of user interface devices coupled to the relatively low speed bus.

9. The computer system of claim 7 wherein the relatively low speed bus comprises an industry standard architecture ("ISA") bus.

10. The computer system of claim 1 wherein the memory device is programmable by the CPU so that the CPU can transfer information to and store the information in the memory device.

11. The computer system of claim 1 wherein the memory device is programmable by the CPU so that the CPU can transfer information to and store the information in the memory, and wherein the computer system further comprises a prompting device and a disk drive unit adapted to receive a disk containing digital information, the prompting device and the disk drive unit being coupled to the CPU, and wherein the crisis recovery routine causes the CPU to activate the prompting device to prompt for a disk containing the alternative BIOS program for the CPU to be placed in the disk drive, and to transfer the alternative BIOS program to the memory device.

12. The computer system of claim 11 wherein the startup program contained in the memory device causes the CPU to compare the system data to BIOS identifying data corresponding to the alternative BIOS program, and in the event the system data and the BIOS identifying data corresponding to the alternative BIOS program do not correspond to each other, provides a user perceivable indication.

13. The computer system of claim 1 wherein the memory device contains a plurality of BIOS programs and corresponding BIOS identifying data, and wherein the startup program stored in the memory device causes the CPU to read the system data and the BIOS identifying data from the memory device, compare the system data to the BIOS identifying data, and, in the event the system data matches BIOS identifying data corresponding to one of the BIOS programs, causes the CPU to execute the corresponding BIOS program.

14. The computer system of claim 13 wherein, in the event the system data does not match the BIOS identifying data corresponding to any of the BIOS programs, the startup program stored in the memory device causes the CPU to execute the crisis recovery routine.

15. The computer system of claim 1 wherein the first circuit component further comprises a programmable array logic device, and wherein the system data is stored in the programmable array logic device.

16. The computer system of claim 1 wherein the BIOS program, the BIOS identifying data, and the start-up program are stored in the same integrated circuit device.

17. The computer system of claim 1 wherein the system data identifies the type of CPU in the first circuit component.

18. A computer system comprising:

a central processing unit ("CPU");

a storage device containing system data identifying hardware or software in the computer system;

a memory device separate from the storage device, the memory device containing a basic input/output system ("BIOS") program, BIOS identifying data corresponding to the BIOS program, and a startup program adapted to be executed by the CPU to cause the CPU to read the system data from the storage device and the BIOS identifying data from the memory device, compare the system data to the BIOS identifying data, and, in the event the system data and the BIOS identifying data do not correspond to each other, cause the CPU to automatically execute a crisis recovery routine that allows loading of an alternative BIOS program.

19. The computer system of claim 18 wherein the memory device is programmable by the CPU so that the CPU can transfer information to and store information in the memory device.

20. The computer system of claim 18 wherein the additional routine comprises a crisis recovery routine.

21. The computer system of claim 18 wherein the memory device is programmable by the CPU so that the CPU can transfer information to and store the information in the memory device, and wherein the computer system further comprises a prompting device and a disk drive unit adapted to receive a disk containing digital information, the prompting device and the disk drive unit being coupled to the CPU, and wherein the crisis recovery routine causes the CPU to activate the prompting device to prompt for a disk containing the alternative BIOS program to be placed in the disk drive, and transfers the alternative BIOS program to the memory device.

22. The computer system of claim 21 wherein the prompting device comprises a display monitor.

23. The computer system of claim 18 wherein the storage device comprises a programmable array logic device programmed with the system data.

24. The computer system of claim 18 wherein the memory device contains a plurality of BIOS programs and corresponding BIOS identifying data, and wherein the startup program stored in the memory device causes the CPU to read the system data from the storage device and the BIOS identifying data from the memory device, compare the system data to the BIOS identifying data, and, in the event of a match, causes the CPU to execute the BIOS program.

25. The computer system of claim 24 wherein, in the event the system data does not match the BIOS identifying data corresponding to any of the BIOS programs, the startup program stored in the memory device causes the CPU to execute the crisis recovery routine.

26. The computer system of claim 18 wherein the storage device comprises a programmable array logic device storing the system data.

27. The computer system of claim 18 wherein the memory device in which the BIOS program, the BIOS identifying data, and the start-up program are stored comprise a single integrated circuit device.

28. The computer system of claim 18 wherein the system data identifies the type of CPU in the computer system.

29. A computer system comprising:

a daughterboard including a central processing unit ("CPU") having a CPU bus, a system memory, a relatively high speed bus, a system controller coupling the CPU bus to the system memory and to the relatively high speed bus, and a storage device coupled to the relatively high speed bus, the storage device containing CPU data identifying the CPU; and

a motherboard removably receiving the first circuit board, the motherboard including a relatively high speed bus coupled to the relatively high speed bus of the daughterboard, a relatively low speed bus, a bus bridge coupling the relatively high speed bus to the relatively low speed bus, and a memory device coupled to the relatively low speed bus containing a basic input/output system ("BIOS") program, BIOS identifying data identifying the CPU that is adapted to execute the BIOS program, and a startup program adapted to be executed by the CPU to cause the CPU to read the CPU data from the storage device and the BIOS identifying data from the memory device, compare the CPU data to the BIOS identifying data, and, in the event the CPU data and the BIOS identifying data do not correspond to the same CPU, cause the CPU to automatically execute a crisis recovery routine that allows loading of an alternative BIOS program.

30. The computer system of claim 29 wherein the memory device containing the BIOS program, the BIOS identifying data, and the startup program comprise a single integrated circuit.

31. The computer system of claim 27 wherein the relatively high speed bus comprises a peripheral connect interface ("PCI") bus.

32. The computer system of claim 29 further comprising a plurality of user interface devices coupled to the relatively low speed bus.

33. The computer system of claim 29 wherein the relatively low speed bus comprises an industry standard architecture ("ISA") bus.

34. The computer system of claim 29 wherein the memory device is programmable by the CPU so that the CPU can transfer information to and store the information in the memory device.

35. The computer system of claim 29 further comprising a prompting device and a disk drive unit adapted to receive a disk containing digital information, the prompting device and the disk drive unit being coupled to the CPU, and wherein the crisis recovery routine causes the CPU to activate the prompting device to prompt for a disk containing the alternative BIOS program for the CPU to be placed in the disk drive, and transfers the alternative BIOS program to the first memory device.

36. The computer system of claim 35 wherein the startup program contained in the memory device causes the CPU to compare the CPU data to data identifying the CPU corresponding to the alternative BIOS program, and in the event the CPU data and the data identifying the CPU corresponding to the alternative BIOS program do not correspond to the same CPU, provides a user perceivable indication.

37. The computer system of claim 29 wherein the storage device comprises a programmable array logic device programmed with the CPU data.

38. The computer system of claim 29 wherein the memory device contains a plurality of BIOS programs and corresponding BIOS identifying data identifying a respective CPU that is adapted to execute each BIOS program; and wherein the startup program stored in the memory device causes the CPU to read the CPU data from the storage device and the BIOS identifying data from the memory device, compare the CPU data to the BIOS identifying data, and, in the event the CPU corresponding to the CPU data matches a CPU corresponding to one of the BIOS programs, causes the CPU to execute the BIOS program.

39. The computer system of claim 38 wherein, in the event the CPU corresponding to the CPU data does not matches a CPU corresponding to any of the BIOS programs, the startup program stored in the second memory device causes the CPU to execute the crisis recovery routine.

40. A daughterboard for a computer system having a motherboard which is adapted to removably receive the daughterboard, the motherboard containing a memory device containing a basic input/output system ("BIOS") program, BIOS identifying data corresponding to the BIOS program, and a startup program, the daughterboard comprising a central processing unit ("CPU") and a storage device containing hardware data identifying at least one hardware component on the daughterboard, the startup program stored in the memory device being adapted to be executed by the CPU to cause the CPU to read the hardware data from the storage device and the BIOS identifying data from the memory device, compare the hardware data to the BIOS identifying data, and, in the event the hardware data and the BIOS identifying data do not correspond to the same hardware component, cause the CPU to automatically execute a crisis recovery routine that allows loading of an alternative BIOS program.

41. The daughterboard of claim 40 wherein the CPU includes a CPU bus, and wherein the daughterboard further comprises a system memory and a system controller specifically adapted to interface with the CPU, the system controller coupling the CPU bus to the system memory.

42. The daughterboard of claim 40 wherein the CPU includes a CPU bus, and wherein the daughterboard further comprises a PCI bus and a system controller specifically adapted to interface with the CPU, the system controller coupling the CPU bus to the system memory and to the PCI bus.

43. The daughterboard of claim 40 wherein the storage device comprises a programmable array logic device programmed with the hardware data.

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